

CLAIMS

What is claimed is:

1. A method of forming an interconnect between a first layer copper line and a second layer copper line of a semiconductor circuit, said method comprising:

forming a via through a first dielectric layer to expose the surface of the first layer copper line;

depositing a first barrier layer over inner sidewall and bottom surfaces of the via, the barrier layer providing a diffusion barrier against copper;

etching selectively the bottom surface of the via to substantially eliminate the barrier layer from the bottom surface; and

depositing a second barrier layer over the inner surfaces of the via, the second barrier layer providing a diffusion barrier against copper and ensures sufficient wettability of copper.

2. The method of claim 1 further comprising forming a trench in the dielectric layer, a portion of which lies substantially over the via; wherein the first and second barrier layers are deposited on inner surfaces of the trench.

3. The method of claim 1 further comprising the step of depositing copper in the inner surfaces of the via and trench, thereby substantially filling the via and trench with the deposited copper.

4. The method of claim 1 wherein the first barrier layer is a conformal barrier layer.
5. The method of claim 4 wherein the conformal barrier layer is a layer of plasma+silane treated CVD TiNSi.
6. The method of claim 4 wherein the conformal barrier layer is an ALD layer of TaN.
7. The method of claim 1 wherein the first barrier layer is an ionized PVD layer of at least one of the following materials: Ta, TaN.
8. The method of claim 1 wherein the first barrier layer comprises at least one of the following materials: TiNSi, Ta, TaN, TaSiN, Ti, TiN, W, WN, WSiN, WCN, and Ru.
9. The method of claim 1 wherein the selective etching is performed in a PVD barrier chamber.
10. The method of claim 1 wherein the second barrier layer is a flash PVD layer of Ta.
11. The method of claim 1 wherein the flash barrier layer is a PVD layer of Ta and wherein depositing the second barrier layer is performed in the same PVD barrier chamber as the selective etching.
12. The method of claim 1 wherein the second barrier layer has lower resistivity with respect to the first barrier layer.
13. A stacked interconnect structure for coupling a first layer copper line with a second layer copper line comprising:

a via extending through a first dielectric layer to expose the surface of the first layer copper line, the via having an inner core comprising copper;

a first barrier layer covering substantially vertical and bottom surfaces of the inner core; and

a second barrier layer substantially covering the vertical surfaces and not the bottom surface of the via, the second barrier layer lying between the first barrier layer and the first dielectric layer; and

wherein the second barrier layer provides a diffusion barrier against copper and the first barrier layer provides a barrier to copper, ensures wettability of the copper, and is relatively lower in resistivity than the second barrier layer.

14. The structure of claim 13 wherein a top surface of the via is coupled to a portion of the second layer copper line.

15. The structure of claim 13 wherein the second barrier layer is a conformal barrier layer.

16. The structure of claim 15 wherein the conformal barrier layer is a layer of plasma+silane treated CVD TiNSi.

17. The structure of claim 15 wherein the conformal barrier layer is an ALD layer of TaN.

18. The structure of claim 13 wherein the second barrier layer is an ionized PVD layer of at least one of the following materials: Ta, TaN.

19. The structure of claim 13 wherein the second barrier layer comprises at least one of the following materials: TiNSi, Ta, TaN, TaSiN, Ti, TiN, W, WN, WSiN, WCN, and Ru.
20. The structure of claim 13 wherein the first barrier layer is a flash PVD layer of Ta.
21. The structure of claim 13 wherein the flash barrier layer is a PVD layer of Ta and wherein depositing the second barrier layer is performed in the same PVD barrier chamber as the selective etching.